

**REMARKS**

Section A addresses the drawing objections of the office action of January 25, 2006. Section B lists the current status of the claims. Sections C through I address the claim rejections and objections in the order in which they appear in the January 25 office action.

**A. Drawing Objections**

The Examiner objected that not every claimed feature appears in the drawings. The Examiner objected to the absence of elements a)-k) in paragraph 6 of the office action of January 25. Applicants have attempted to address each objection.

Regarding elements a)-e), new drawing figure Fig. 11 shows a substrate device level L1, a first above-substrate device level L2, the pitch P2 of the first above-substrate device level less than the pitch P1 of the substrate device level L1. The substrate device level L1 includes driver circuitry C, while the first above-substrate device level L1 includes memory cells M. The subject matter of Fig. 11 is fully described in the specification, for example at paragraphs [0006]-[0011], [0032]-[0034], and [0037]-[0040], *inter alia*; thus Fig. 11 does not constitute new matter. New paragraph [0037.1] refers to elements of Fig. 11, and similarly does not constitute new matter.

Regarding element f), Applicants respectfully submit that Fig. 4 illustrates a first area (the dense area in the center of the figure) of memory cells having the first above-substrate pitch, and the second area having a fan-out pitch (the less dense area at the far left and right of the figure), the fan-out pitch larger than the above-substrate pitch. Regarding element g), the die including dummy structures, claim 9 has been cancelled.

Regarding element h), Fig. 11 further shows a second above-substrate level L3 formed above first above-substrate device level D2. Additional memory levels above a first memory level are described in, for example, paragraphs [0033] and [0038], and Figs. 10a and 10b illustrate additional stacked memory levels having the same pitch as a first memory level.

Regarding element j, the elements of claim 13 (segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line) are illustrated in new Fig. 12, and described in new paragraphs [0072.1]-[0072.5]. This figure and these paragraphs are drawn from United States Patent Application No. 10/403752, which was incorporated by reference at paragraph [0072], and thus do not constitute new matter. Claim 14 has been cancelled.

Regarding element k, the elements of claim 18 (memory cells arranged in series-connected NAND strings) are illustrated in new Fig. 13, and described in new paragraphs [0070.1]-[0070.6]. This figure and these paragraphs are drawn from Scheuerlein et al., US Patent Application No. 10/335078, which was incorporated by reference at paragraph [0030], and thus do not constitute new matter.

#### **B. Status of the Claims**

Claims 1-59 are pending in the application. Claims 19-59 are withdrawn from consideration. Claims 1-3, 12, 15 and 16 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al., US Patent No. 6,631,085 in view of Owada et al., US Patent No. 5,060,045. Claims 4-10 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Cleaves et al., US Patent No. 6,486,066.

Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Mitsubishi Electric, Japanese Publication No. 3393923. Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Pio, US Patent Application Publication No. 2003/0192101. Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Young, US Patent No. 5,621,683. Claim 18 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al., Young, and Nakai, US Patent No. 5,587,948.

Claim 11 was objected to as being dependent upon a rejected base claim, but was considered allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**C. 35 USC 103(a) Rejections: Claims 1-3, 12, 15 and 16**

Claims 1-3, 12, 15 and 16 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al.

Claim 1 recites a semiconductor die comprising: a substrate device level having a substrate pitch; and a first above-substrate device level formed above the substrate device level, the first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch.

The Examiner finds these elements in Kleveland et al., except that Kleveland fails to disclose that the first above-substrate pitch is smaller than the substrate pitch. The Examiner finds an above-substrate device level in Owada et al. as described in the Abstract, and asserts:

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a first above-substrate device level having a first above-

substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch as disclosed in Owada because it aids in increasing the versatility of the wiring ...

Applicant respectfully suggests, however, that while Owada et al. teach a smaller second wiring level pitch above a first wiring level pitch, this teaching offers no guidance relevant to selecting the relative pitches of two stacked *device levels*.

A device level is a plurality of devices formed at substantially the same height in or above a substrate. A plurality of CMOS devices formed in a substrate may form a substrate device level, for example, where the gate pitch defines the substrate device level pitch. A plurality of memory cells formed above the substrate, for example in a memory array, may form an above-substrate device level, and these memory cells will be formed at an above-substrate pitch. These memory cells may be antifuse-diode or charge storage memory cells, for example.

Kleveland et al. do indeed teach an above-substrate device level formed above a substrate device level. Kleveland et al. do not teach the above-substrate device level formed at a smaller pitch than the substrate device level.

The smaller pitches in the above-substrate levels of Owada et al. are found in *wiring* levels, not device levels, and Owada et al. describe schemes of arranging connectivity to devices, where the devices are formed in the substrate only. Wiring has one simple function, to provide electrical connectivity.

Devices have a very different function, to perform as logic or memory, for example. Devices generally have much more complex structure than wiring, and are substantially more complex to fabricate. Applicants respectfully suggest that any teaching regarding the spacing of wiring in a wiring level is of no relevance to how devices in a device level can or should be spaced. The Examiner's suggested motivation,

in fact, as described in Owada et al., is “to increase the versatility of the wiring” (col. 4, lines 7-24 of Owada et al.); as the claim recites the relative pitches of *device* levels, rather than wiring levels, it is unclear how this motivation can apply.

Applicants believe that since Owada et al. offer no teaching regarding selecting pitch in an above-substrate device level, the suggested combination cannot be considered obvious, and respectfully request reconsideration.

**D. 35 USC 103(a) Rejections: Claims 4-10**

Claims 4-10 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Cleeves et al.

Claims 4-8 and 10 depend from claim 1. As described in Section C of these remarks, the teachings of Owada et al. do not render the suggested modification of Kleveland et al. obvious. Thus claim 1 and its dependent claims distinguish over the suggested combination.

Claim 9 has been cancelled

**E. 35 USC 103(a) Rejections: Claim 13**

Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Mitsubishi Electric.

Claim 13 depends from claim 1. As described in Section C of these remarks, the teachings of Owada et al. do not render the suggested modification of Kleveland et al. obvious. Thus claim 1 and its dependent claims distinguish over the suggested combination.

**F. 35 USC 103(a) Rejections: Claim 14**

Claim 14 has been cancelled.

**G. 35 USC 103(a) Rejections: Claim 17**

Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Young.

Claim 17 depends from claim 1, and adds the limitations that the first above-substrate device level comprises memory cells, wherein the memory cells are thin film transistors having a charge-storage dielectric. The memory cells of Young (see Fig. 2 of Young, for example) are clearly much more complex to form than the wiring levels of Owada et al. Applicants can discern no motivation to replace the above-substrate memory cells of Kleveland et al. with the cells of Owada et al., and then to form these cells at the small wiring pitches of Owada et al.; Applicants will further maintain that no teaching found in these three applications teaches how such an array of these more complex memory cells is to be formed at such a pitch.

Applicants will assert that the references cannot be combined as suggested, and respectfully request reconsideration.

**H. 35 USC 103(a) Rejections: Claim 17**

Claim 18 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al., Young, and Nakai.

Claim 18 depends from claim 17, adding the limitation that the memory cells are arranged in series-connected NAND strings.

Section G of these remarks explained that the suggested combination of Kleveland et al., Owada et al., and Young et al. is neither obvious nor practicable, and thus claim 17 cannot be considered obvious over these references. Dependent claim 18

thus is also not obvious over the suggested combination, and Applicants respectfully request reconsideration.

**I. Claim objections: Claim 11**

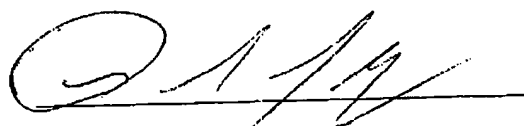
Claim 11 was objected to as being dependent upon a rejected base claim, but was considered allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the indication of allowable subject matter.

**CONCLUSION**

In view of the preceding Remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicants **respectfully request an interview**. In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

May 24, 2006

Date



Pamela J. Squyres  
Agent for Applicants  
Reg. No. 52246

Pamela J. Squyres  
SanDisk Corporation  
3230 Scott Blvd  
Santa Clara, CA 95054  
Tel. 408-869-2921